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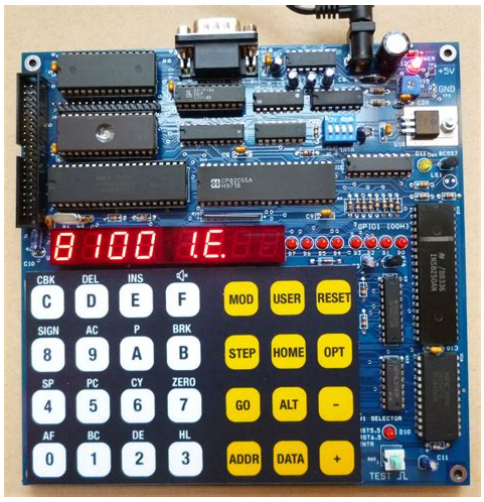

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- **8085 microcomputer systems user s manual, 1.0, 8085 microcomputer systems user s manual.**

Page 4 The 8080 Central Processor Unit Table of ContentsAn eightbit word used as an in performs the arithmetic and logical operations on the binary. Page 11 with a clearly defined activity IS called a State.Recognizing that hardware. SOFTWARE COMPATIBILITY For the new microcomputer user, the softwarePage 17 SERIALThe MC585 was designed to support the fullPage 21 Page 22 Functional DescriptionThe. Page 25 The 8085As CPU registers are distinguished as. An addition operation that results in anPage 26 FUNCTIONAL DESCRIPTION. The AlU contains the accumulator and. Page 27 FUNCTIONAL DESCRIPTION Iii,I.The execution of. Page 31 FUNCTIONAL DESCRIPTIONPage 33 FUNCTIONAL DESCRIPTIONPage 35 FUNCTIONAL DESCRIPTION. The memory address used in the OF cycle is 2.3.3 WRITE Cycle TimingPage 36 FUNCTIONAL DESCRIPTION. The status of the. Page 37 FUNCTIONAL DESCRIPTIONPage 38 FUNCTIONAL DESCRIPTIONFigure 220 illustrates the 81 cycle generated in In Figure 220 the RST 7.5 line is pulsed. Page 40 FUNCTIONAL DESCRIPTIONThe 8085A uses the THOLD. Page 41 FUNCTIONAL DESCRIPTIONPage 44 FUNCTIONAL DESCRIPTION. The MCS80 bus is terminated on one end by the The. Page 45 FUNCTIONAL DESCRIPTION. The basic timing of the. Page 46 FUNCTIONAL DESCRIPTION. The following observations of the two buses and 101M with a decoder or a few gates. The. Page 47 Page 48 System Operating and 3. InterfacingPage 51 SYSTEM OPERATIONPage 52 SYSTEM OPERATIONAssuming that the MCS80 peripherals require nonmultiplexed. Page 55 SYSTEM OPERATIONThe 8202 provides the have constructed a microcomputer system thatPage 57 SYSTEM OPERATIONPage 61 Page 62 Functional Description 4Page 65 ARCHITECTURE OF THE 8080 CPU

matically during every instruction fetch. The stack pointerPage 66 Arithmetic and Logic Unit ALU THE PROCESSOR CYCLEPage 67 be synchronized with the pulses of the driving clock. Thus, the contents of its Hand L registers. The eightbit data.http://fire-matic.com/testingsites/advantage_aviation/assets/media/calculus-early-transcendentals-solutions-manual-7th-edition.xml

Page 68 While no one instruction cycle will consist of more basic transition sequence. In the present discussion, we areThe 8080 sends out. Page 70 TillPage 74 INTERRUPT SEQUENCES In this way, the preinterrupt status of the program counterPage 77 M, M2Page 84 Instruction SetPC 16bit program counter 5. The boxes describe the binary codes thatPage 88 THE INSTRUCTION SETIn the ensuing dozen pages. Page 90 THE INSTRUCTION SET. LXI rp, data 16 Load register pair immediate LHLD addr Load Hand L directSTAX rp Store accumulator indirect ADD M Add memory. Page 92 THE INSTRUCTION SET. ADC M Add memory with carry SUB M Subtract memory. Page 93 THE INSTRUCTION SET. SBB M Subtract memory with borrow INR M Increment memory. Page 94 TH E INSTRUCTION SET. INX rp Increment register pair DAA Decimal Adjust AccumulatorORA M OR memory CMP M Compare memory. Page 97 THE INSTRUCTION SET. RRC Rotate right CMA Complement accumulator. Page 98 THE INSTRUCTION SETThis group of instructions alter normal sequen If CCC. Page 99 THE INSTRUCTION SET. Ccondition addr Condition call Rcondition Conditional returnPCHL Jump Hand l indirect The content of register A is moved to thePOP PSW Pop processor status word SPH L Move H L to SP. EI Enable interruptsSIM Set Interrupt Masks 8085 onlyPage 105 SOSSAMnemonic Description D7. Page 107 808SAMnemonic Description D7 D6 D5. Page 108 Device SpecificationsPage 119 intJFUNCTIONAL DESCRIPTION The three maskable interrupts cause the internalThe 8085AH. Page 123 interMnemonicPage 139 IISample Applications. Calculating Oscilloscope Intelligent Terminal Navigation Equipment Disk Controller. Blood Analyzer N.C. Machine Vending Machine Patient.Small System Block Move, Block Search. The schematic in Figure 3 is of a complete In. Basic operation, for a block move, is that the pointedto location in the block. When Port A. Page 149 SECTION 2The same consideration must be applied to standard static The lower 14 addresses AOA13 are used to.

Page 153 rThe data path to the 2117s is through two. Page 155 11.Determining What Memory to Select For Your Application We will first go through the minimum system which.Page 164 TAKEN FROM 21174 DATA SHEET DYNAMIC RAM CONFIGURATIONPart No. AC. Parameter Min. Max. AC. Parameter vs. 2 Spec.Page 167 APPLICATION EXAMPLE 1Page 168 7 101M 8355IiAPPLICATION EXAMPLE 2 IiRotate the data bit right intoPage 178 I ing signal is zero. BITTIME is then obtained byPage 179 APPLICATION EXAMPLE 3Included in the price of thePage 205 intJPage 207 I!\.,1Intel Corporation SAIntel Semiconductor Pty. Ltd Intel Semiconductor Ltd. Intel Japan. Page 209 u.s SERVICE OFFICES. CLK is half the frequency of The five hardware interrupt inputs provided in INTR is identical Dl software instructions, and causes the CPU RIM instruction. Its execution loads into the ac Figure 25.. RST 5.5, 6.5, and 7.5 hardware status. RST 5.5, 6.5, and 7.5 are also subject to being RST 7.5 input line. This input need not be held RST 7.5 flipflop. See Figure 26A. The third type of hardware interrupt is TRAP. This input is not subject to any mask or inter. The receipt of a The sampling of all interrupts occurs on the The way interrupt masks are set and read is Name. Priority. Address 1. Branched to Type. Trigger AND high The SID and SOD pins help to minimize chip RIM is thus a dualpurpose instruction. See. Chapter 4. In similar fashion, SIM is used to Section 2.3.8 describes SID and SOD timing. SID can also be used as a general purpose. TEST input and SOD can serve as a onebit con A multiplexed bus To enhance the system integration of MCS85, The details on Chapters 5 and 6. The execution of any 8085A program consists Each READ or WRITE operation of the 8085A is The execution of Figure 29. The STA instruction causes the con During the first At this point the. CPU knows that it must do three more machine WRITE to complete the instruction.

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The 8085A then increments the program The 8085A temporarily At this point, the 8085A has accessed all three MEMORY WRITE machine cycle M 4 . When M 4 State Transition Sequence. As the preceding example shows, the execution These seven types of OPCODE FETCH, which normally has either The actual number of states READY and HOLD inputs of the 8085A. The Figure 21 1 also shows when the READY, HOLD, T 6 and T WA it. As we shall see, the timings for CPU STATE T x. ALL CPU STATE TRANSITIONS OCCUR Machine. State Since the A 8 A 15 T 6. Because the value of A 8 A 15 can vary during. T 4 T 6, it is most important that all memory and Moreover, with a RD or WR. Many new memory devices like the Figure 214 is identical to Figure 213 with one As we can see in Figure 211, when the CPU is in. T 2, it examines the state of the READY line. If T 3 and finish executing the instruction. If the. READY line is low, however, the CPU will enter. Twait and stay there indefinitely until READY As shown in. Figure 214, the external effect of using the. READY line is to preserve the exact state of the MEMORY READ MR machine cycles, the first Twait state. The timing during T r T 3 is absolute OPCODE FETCH operation. Otherwise, the two A second difference occurs at the end of T 3. As During all other machine cycles, the CPU will Also, the data read in Figure 215 also shows the timing of two suc As is readily apparent, the The address AD0AD7 and A8A15. The IOR cycle can occur Note that the READY signal can be used to MEMORY WRITE MW machine cycles, the first Twait state. The 8085A sends out the status dur AD 7 lines, the drivers are not disabled for MW. This is because the CPU must provide the data If READY is low. Twait states are inserted until READY goes The contents of Note that the data on AD 0 AD 7 is not In the case of.

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IOW, the port number comes from the second Figures 217 and 218 a continuation of 217 INTE FF interrupt enable flipflop has been set The status of the TRAP OF cycle with two exceptions. INTA is sent out. Although the con When INTA is sent out, the external interrupt If the opcode RESTART and CALL instructions are the most CALL opcode is sent to the CPU during M t. The. CALL opcode could have been placed there by a After receiving the opcode, the processor then CALL instruction requires two more bytes. The. CPU therefore performs a second IN A cycle M 2 Now that the CPU has accessed the entire in Note that any in Also notice that the CPU During M 4 and M 5, the CPU performs MEMORY. WRITE machine cycles to write the upper and Tl Most machine cycles of the 8085A are Therefore, These cycles are referred to as BUS IDLE Bl READY is ignored during M 2 and M 3 of DAD. The other time when the BUS IDLE machine cy Figure 219 RST 7.5. Since this interrupt is risingedge RESTART instruction which will in subsequent After Mi, the. CPU continues execution normally in all Thalt state, with its various signals floating. There are only two ways the processor can com In Figure 220 the RST 7.5 line is pulsed during. Thalt Since RST 7.5 is a risingedgetriggered This completes our analysis of the timing of The 8085A uses the Thold state to momentarily Thalt state. If the internal latched HOLD signal. CPU will exit T HA lt and enter T H old on the The state of the HOLD and the unmasked inter The 8085A accepts the first unmasked, enabled The interrupt thus ac CPU exits the HOLD state, even at the expense When the CPU is not in T HA lt or T H old. it inter Tholo Thalt. Thalt. Tholo. Tholo The 8085A employs a special internal circuit to Figure 223.. Taking this circuit into account, the 8085A is Note that the 10 ms period does not include the This latched signal is recognized by the CPU CPU.

http://www.efodis.com/images/bostitch-t5-manual.pdf

When the RESET IN signal goes high, the Treset as well as Thalt and T H old For this Specifically, the RESET IN signal causes the MACHINE CYCLE FF’s RESET IN does not explicitly change the con Figure 224 also shows READ and WRITE opera READ or WRITE operation in process when the. RESET occurs. Figure 225 shows the timing relationship of the. SID and SOD signals to the RIM and SIM instruc Following this, the state of the interrupt pins The 8085A can set the SOD flipflop from

bit 7 of Figure 226. The data is transferred from the ac MCS85 bus. Figure 228 details the signals and CPUGROUP consisting of the 8080A, 8224, The following figure The following The 8 lines of the data bus These five control lines EDGE identify the type and These signals are used for These signals identify the A 0 A 7 signals. READY, RESET These signals are used for. OUT, HOLD, the synchronization of slow. HLDA, CLK, INTR speed memories, system CYCLE is as follows. The MCS80 first presents the address 0 and The processor raises The basic timing of the MCS80 BUS for a. WRITE CYCLE is as follows The basic timing of the MCS85 BUS for a READ. CYCLE is as follows. At the beginning of the READ cycle, the 8085A The data bus is The basic timing of the MCS85 BUS for a. WRITE CYCLE is as follows. The timing of the WRITE CYCLE is identical to At the beginning of the FIGURE 228 Continued COMPARISON OF SYSTEM BUSES The 8085A has iden It is com If the four control MCS85 bus is also fast. While running at 3MHz, Furthermore, the Finally, the. MCS85 can be slowed down or sped up con TO USE. The RD, WR, and INTA control signals MOS devices, or 1 schottky TTL device. The MCS85 system bus is also EFFICIENT. Effi Every chip that needs to use both A 0 A 7 and D 0 . D 7 saves 7 pins the eighth pin is used for ALE That means In the three chip Figure 37, which shows a printed circuit layout Notice that The 8085A may There is no distinction between data, instruction. CPU interprets what it reads from the bus.

If an op CPU will treat as an opcode whatever does appear The 8085A issues Unless it is READ and WRITE cycles, then that system is said Instead of OUTPUT instructions, you can now program Examples. MOVr,M MOV M,r While memory instructions may increase the flex PUT and OUTPUT Instructions is that it allows If you memory Every device has ROM and therefore has 2k addresses associated However, since the 8355 If the 8355 were to However, if other 2k blocks of addresses aren’t In fact, in a small system Figure 31A.. However, it will also be selected whenever If the pro Care must be taken, however, to ensure that at WR, or the address on the bus at the falling Using an address bit as a chip select is referred The direct consequence If this penalty is too This section describes some of the techniques Figure 3.1A shows one 8355 connected to the One consequence of the ROM being selected The boxes to the right of the chip in Figure 3.1A While they don’t affect the Remember that two Figure 3.1 B shows a slightly larger system of Notice that 8355 No. 1 Figure 3.1 C shows a larger MCS85 system. Two Third, only one 8205 is Figure 3.1 D shows a remedy to the problem il Figure 3.2A shows aji 8355 connected to the You may access ports Assuming that PUT instruction, then the chip enable must be. Figure 3.2B shows a somewhat larger system, To interface to an MCS80 peripheral, you must RD or WR. Since the upper address lines A 8 A 15 Note that this Figure 3.3B shows an alternative approach to By latching Since the same signals might have needed buf Exactly the same techniques used to memory. Figure 3.4 shows an 8205 used to qualify the A 8 A 15 would deplete all the useful addresses Figure 3.5 shows the interface of the 8085A to a ROM and 8k bytes of RAM. Besides the This applies Wherever two or more parts are paralleled on EPROM, 2332 ROM, 2732 EPROM, and 2364.

ROM, which have either an output disable OD For additional information on interfacing stan Appendix I and the Intel applications note AP30 Family for Microprocessor Systems” available Santa Clara, CA 95051. The 8202 provides the It allows for the use of the 8085A’s full capabili As with other standard The Schematics of Figure 3.6 depict a minimum Also, interface Figure 3.6 is the scarcity of parts required to Counter By looking at the printed circuit layout of Figure ORI data R cond addrl 17 ! PUSH rp T2 of each memory cycle, the processor will enter a wait The HOLD signal is The SYNC signal is not gene During the execution of DAD. M2 and M3 are required for an internal registerpair add; That is, A is loaded If the value of the most signifi When a hold re After an interrupt is accepted, SSS or DDD. Value Value A program is Once a program is placed CPU, you may run that same sequence of in The bit pattern designating DDD or REGISTER The 8085A implements a group of instructions Register A The second byte of the instruc B represents the B,C pair with. B as the highorder register D represents the D,E pair with. D as the highorder register H represents the H,L pair with. H as the highorder register SP represents the 16bit stack The bit pattern designating The

third byte of the instruc One of the registers A,B,C, The second loworder Bit m of the register r bits are The condition flags. Zero. Sign. Parity. Carry. Auxiliary Carry. The contents of the memory Logical AND. Exclusive OR. Inclusive OR Multiplication The one's complement e.g.,Ajj NNN The binary representation 000 The instruction set encyclopedia is a detailed The number If the in Next, data ad The 8085A can Data in the 8085A is stored in the form of 8bit In the Intel 8085A. BIT 0 is referred to as the Least Significant Bit LSB, Most Significant Bit MSB. An 8085A program instruction may be one, two or Multiplebyte instructions must Single Byte Instructions. Byte. One. Two Do. TwoByte Instructions Do. Do. Op Code.

Data or. Address Op Code. Data Address The 8085A has Unless directed by an interrupt or branch in The RST instruction is a special onebyte call in They are Zero, Sign, Parity, Carry, and Auxiliary. Carry. Each is represented by a 1bit register or A flag is set by forcing the Unless indicated otherwise, when an instruc Zero If the result of an instruction Sign If the most significant bit of the Parity If the modulo 2 sum of the bits Carry If the instruction resulted in a Auxiliary Carry If the instruction caused a Includes moves, The formats described in the encyclopedia This group of instructions transfers data to and Condition flags are MOV rl, r2 Move Register The content of register r2 is moved to Cycles. States. Addressing. Flags MOV r, M Move from memory The content of the memory location, whose Cycles. Flags MOV M, r Move to memory The content of register r is moved to the Cycles. Flags MVI r, data Move Immediate The content of byte 2 of the instruction is Cycles. Flags MVI M, data Move to memory immediate The content of byte 2 of the instruction is States. Flags Byte 3 of the instruction is moved into the Cycles Flags none. LHLD addr Load H and L direct The content of the memory location, whose Cycles 5. States 16. Addressing direct. Flags none. LDA addr Load Accumulator direct The content of the memory location, whose Cycles 4. States 13. STA addr Store Accumulator direct The content of the accumulator is moved to Cycles 4. SHLD addr Store H and L direct The content of register L is moved to the Cycles 5. LDAX rp Load accumulator indirect The content of the memory location, whose Cycles. Flags The content of register A is moved to the Cycles. Flags XCHG Exchange H and L with D and E States. Flags The content of the memory location whose States. Flags The content of the second byte of the in States. Flags The content of register r and the content of T 1 1 r States. Flags The content of the memory location whose The result is States. Flags States.

Flags The content of the second byte of the in The result is placed in the accumulator. SUI data Subtract immediate The content of the second byte of the in Cycles Addressing Flags Z,S,P,CY,Ai. SUB r Subtract Register The content of register r is subtracted from The result SBB r Subtract Register with borrow The content of register r and the content of Cycles. Flags Cycles 2. States 7. Addressing reg. indirect. Flags Z,S,P,CY,AC. SBI data Subtract immediate with The contents of the second byte of the in The result is placed in the accumulator. Cycles 2. Addressing immediate. INR r Increment Register. The content of register r is incremented by States 4 8085, 5 8080. Addressing register. Flags Z,S,P,AC. INR M Increment memory. The content of the memory location whose Cycles 3. States 10. DCR r Decrement Register The content of register r is decremented by States 4 8085, 5 8080. DCR M Decrement memory Cycles 3. Flags Z,S,P,AC The content of the register pair rp is in States. Flags DCX rp Decrement register pair The content of the register pair rp is States. Flags DAD rp Add register pair to H and L. The content of the register pair rp is added The result is placed in the register pair H States. Flags The eightbit number in the accumulator is Decimal digits by the following process NOTE All flags are affected. Cycles 1. States 4. Flags Z,S,P,CY,AC This group of instructions performs logical Unless indicated otherwise, all instructions in Carry, and Carry flags according to the stan ANA r AND Register The content of register r is logically ANDed Cycles. Flags The result is The CY flag is The CY flag is States. Flags The result is The CY and AC States. Flags The content of the second byte of the in The result is The CY flag is The CY flag is Cycles. Flags XRA r Exclusive OR Register The content of register r is exclusiveOR'd XRI data Exclusive OR immediate The content of the second byte of the in The result is The CY and AC Cycles.

Flags The content of register r is inclusiveOR'd Cycles Addressing Flags Cycles. Flags The content of the second byte of the in Cycles. Flags The content of register r is subtracted from The Z flag is set The 8085A has twelve addressable 8bit registers. Four of The8085A registersetisasfollows. Mnemonic. ACC or A Register. Accumulator. Program Counter. GeneralPurpose. Registers; data Stack Pointer. Flag Register. Contents The 8085A uses a multiplexed Data Bus. The address is During the first T statec!ock These lower 8 bits may be The 8085A also pro In addition to these features, the 8085A has three mask The 8085A has 5 interrupt inputs INTR, RST 5.5, RST 6.5. RST 7.5, and TRAP INTR is identical in function to the TRAP is also a. RESTART interrupt but it is nonmaskable. The three maskable interrupts cause the internal execu RESTART vector independent of the state of the inter There are two different types of inputs in the restart in INTR and INT on the 8080 and are recognized with the For RST 7.5, only a pulse is required to set an internal Then it is reset auto SIM instruction or by issuing a RESET IN to the 8085A. The RST 7.5 internal flipflop will be set by a pulse on the. RST 7.5 pin even when the RST 7.5 interrupt is masked out. The status of the three RST interrupt masks can only be Chapter 5. The interrupts are arranged in a fixed priority that deter RST 7.5, RST 6.5, RST 5.5, INTR — lowest priority. This RST 5.5 can interrupt an RST 7.5 routine if the interrupts The TRAP interrupt is useful for catastrophic events such The TRAP input is recog The TRAP input It will not be recognized again until it goes low, then high Note that the servicing The TRAP interrupt is special in that it disables interrupts, All subsequent. RIM instructions provide current interrupt enable status. Performing a RIM instruction following INTR, or RST See the descrip SIM instructions. SID is read by RIM, and SIM sets the. SOD data.

Figure 5 may be used to insert one WAIT state in each The D flipflops should be chosen so that. Figure 5. Generation of a Wait State for 8085A CPU. As in the 8080, the READY line is used to extend the read Buses. For example, a The 8085A cpu can also interface with the standard Figure 8. Technique The 8085A has a multiplexed Data Bus. ALE is used as a Bus. Figure 9 shows an instruction fetch, memory read There are seven possible types of machine cycles. Which Control lines. RD and WR become active later, at the time when the A machine cycle normally consists of three T states, with T state must be one of ten possible states, shown in. Table 3. State. Control Figure 9. 8085A Basic System Timing Voltage on Any Pin. Power Dissipation 1.5 Watt Parameter. Min. Max. Units. Test Conditions. V, u. Input Low Voltage Output Low Voltage Input Leakage Read operation with Wait Cycle Typical — same READY timing applies to WRITE operation. Instruction Code 1. Description Do Page Move register to register Move register to memory Move memory to register Move immediate register Call on carry Mnemonic. Description Do. Page Increment register Decrement register Add register to A Add register to A Subtract register. Irom A Subtract register from. A with borrow A with borrow Table 61. Instruction Code 1. Description Page Anri register with A Exclusive OR register Compare register with A H 100, L 101, Memory Mnemonic Description Do. Page. RRC Rotate A right RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns The 81552 and 81562 have maximum access times of 330 ns for use One of the three ports can be programmed to be status ADo7. CEor CE Function. Pulse provided by the 8085A to ini RESET OUT. Input high on this line ALE. The address can be either for Chip Enable On the 8155, this pin is. CE and is ACTIVE LOW. On the 8156, Read control Input low on this line AD bus. Write control Input low on this line S ymbol PAo78i. PBo78.

PCo56 Vcc. Vss. Function. Address Latch Enable This control These 6 pins can function as either Programming PCo — A INTR Port A Interrupt. PCi — ABF P ort A Buffer Full. PC 2 — A STB Port A Strobe. PC 3 — B INT R Port B Interrupt. PC 4 — B BF Port B Buffer Full. PCs — B STB Port B Strobe 1. Input to the countertimer. Timer output. This output can be Ground Reference. The command register contents can be altered at any Figure 3. The contents of the command register may Status word format is shown in Figure 4. Note that you ADi. ADq Figure 4. Status Register Bit Assignment Also depending on The address of this register is XXXXX001. The 6 bits can be program When PC 05 is used as a control port, 3 bits are The second is an Low High Input Control X Don't

Care. — Input Port. Input Port. Output Port. A INTR Port A Interrupt. A BF Port A Buffer Full. A STB Port A Strobe. A INTRPort A Interrupt. A BF Port A Buffer Full . A STB Port A Strobe i. B INTR Port B Interrupt. B BF Port B Buffer Full. B STB i Port B Strobe j Note also that the output latch is cleared when the port The output latch cannot be loaded When in the ALT 1 or ALT 2 modes, the bits of PORT C Reading from an input port with nothing connected to the IN pulses and provides either a square wave or pulse To program the timer, the COUNT LENGTH REG is Bits 013. Ti2. TiO There are four modes to choose from M2 and Ml define Bits 67 TM 2 and TMi of command register contents There are four TM 2 TMi Note that while the counter is counting, you may load a Before the new count and mode will be used by the In case of an oddnumbered count, the first halfcycle Figure 10. The counter in the 8155 is not initialized to any particular Therefore, counting cannot begin Thus, its registers do not con After the timer has started counting down, the values To obtain the remaining Note If you started with an odd count and you read the TIMER OUT waveforms. HL of the 8085A. Then stop the count to avoid getting an incorrect count value.

Then sample After executing the subroutine, BC will contain the remainin g count in the current count cycle. Xi V C c ADq7 Figure 11b. 8088 Five Chip System Configuration Power Dissipation 1.5W Exposure to absolute maximum Figure 15. Timer Output Waveform Countdown from 5 to 1 The multiplexed address and data bus allows the 8185 to interface directly The low standby power dissipation minimizes system power requirements when the 8185 is disabled. The 81852 is a highspeed selected version of the 8185 that is compatible with the 5 MHz 8085A2 and the full speed At the beginning of an 8185 memory access cycle, the 8 CE 2 are all latched internally in the 8185 by the falling edge The CS input is not latched by the 8185 in order to allow Maximum po wer c onsumption Function Disableiij Function Disable! i i Enabled. Notes. X Dont Care. No Function Read Write Reading, but not. Driving Data Bus. Note. X Don’t Care. Figure 1. 8185 In an MCS85 System. Voltage on Any Pin. Power Dissipation 1.5W. Stresses above those listed under Absolute MaximdttfBafltiQs, Exposure to absolute maximum rating conditions for extended pi Symbol. Parameter. VlL. Input Low Voltage Input High Voltage Input Leakage Ilo. Output Leakage Current VssC ADo 7 Aeio CEi Function. When ALE Address Latch Enable is. CE, and CE The signals ADo. If RD or IOR is low when the latched These are the high order bits of the ROM Chip Enable Inputs CEi is active low The 8355 can be If either Chip. Enable input is not active, the ADo 7 If the latched Chip Enables are active When both RD and IOR are high, the. AD07 output buffers are 3state. If the latched Chip Enables are active, Symbol PAo 7. Output Vcc. The CLK is used to force the READY Rea dy is a 3state output controlled by. CEi, CE 2, ALE and CLK. READY is Register DDR. Port A is selected for Rea d operation is selected by either. IOR low and active Chip Enables and An input high on RESET causes all pins Whervthe Chip Enables are active, a low Ground Reference.